

Atlas-V5 VXS

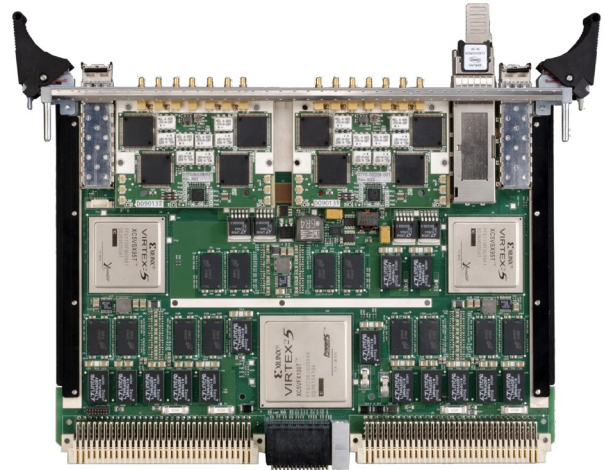
Highest Channel Count/Slot - VXS

First 12-bit 1 Gbps ADC for VXS

Without Compromise

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Features

Benefits

Eight Channels: 12-bit ADC Input at 1 Gbps ea	Latest Available Technologies/Speed Reduces System Size, Saves Money
Sample Accurate Synchronization Across Multiple Boards	Enables Solutions for New Multi-channel Applications
All eight ADCs Clocked from a Common Input, or Two Independent Clock Inputs for Groups of Four ADC channels	Interleaving Applications for Increased Sampling Rate
High Channel Count, Low Latency Data Routing and Large /Fast FPGA Processing	Ideal for Multi-channel Signal Processing Applications such as Beamforming Radar, Space-Time Adaptive Processing (STAP), Direction Finding, Wireless Comms, Sigint, Comint.
Six Digital IO Channels Running at Up to 3.75 Gb/s Using One QSFP and Two SFP+ Front Panel Connections	Flexible Data Movement Across the Front Panel For Use in Standard VME64 Environments
Dual 4x Full Duplex VXS Links and Two Full Duplex VITA 41.6 Ethernet Links	Enhanced VXS Capability
Three Xilinx Virtex®-5 FPGAs: LXT, SXT or FXT for Each Location	Matched FPGA Processing and Analog Data Bandwidth for Dense Channel-count Systems
Three GB DDR3 SDRAM Memory, (one GB per FPGA as 2, 512 MB, 64-bit banks)	Large Memory Resources for Application Flexibility
Advanced Temperature & Current Monitoring	Protection From Damage and Usable in Customer Applications

Overview

The QuiXilica Atlas-V5 VXS is a 6U ANSI/VITA 41 (VXS) compliant high-speed digitizer board that combines high density FPGA processing with four or eight 12-bit ADC input channels performing at 1 Gsps (Gigasamples per second).

By employing three Xilinx Virtex-5 FPGAs, Tekmicro's Atlas-V5 offers unmatched FPGA processing density per channel making it ideal for high channel count signal processing applications.

Atlas-V5 Reduces System Size by 50%

The Atlas-V5 includes eight 1 Gsps analog input channels and three Xilinx Virtex-5 FPGAs, providing up to 2,336 DSP slices and 1.3 TeraMAC/s of signal processing.

The Atlas-V5 features high bandwidth, low latency interconnect paths between its FPGAs. These have been carefully specified to ensure that data from all ADC inputs can be routed to the appropriate FPGA to meet the application processing requirements.

The ADCs are organized as two independent groups of four, each with their own clock and trigger inputs. However, a single clock and a single trigger input may be used for all eight channels on a single board. Synchronization of multiple boards is done using an external trigger signal. This offers significant

throughput advantages for a range of advanced processing algorithms including coherent multi-channel algorithms found in applications such as direction finding, STAP (Space Time Adaptive Processing) RADAR, EW (jamming) and Synthetic Aperture Radar (SAR) Image Formation.

The Atlas-V5 is available for a wide range of operating environments including commercial grade, rugged air, and conduction cooled to support deployed applications such as unmanned airborne, naval and ground vehicles. For more details see Tekmicro's Rugged Data Sheet.

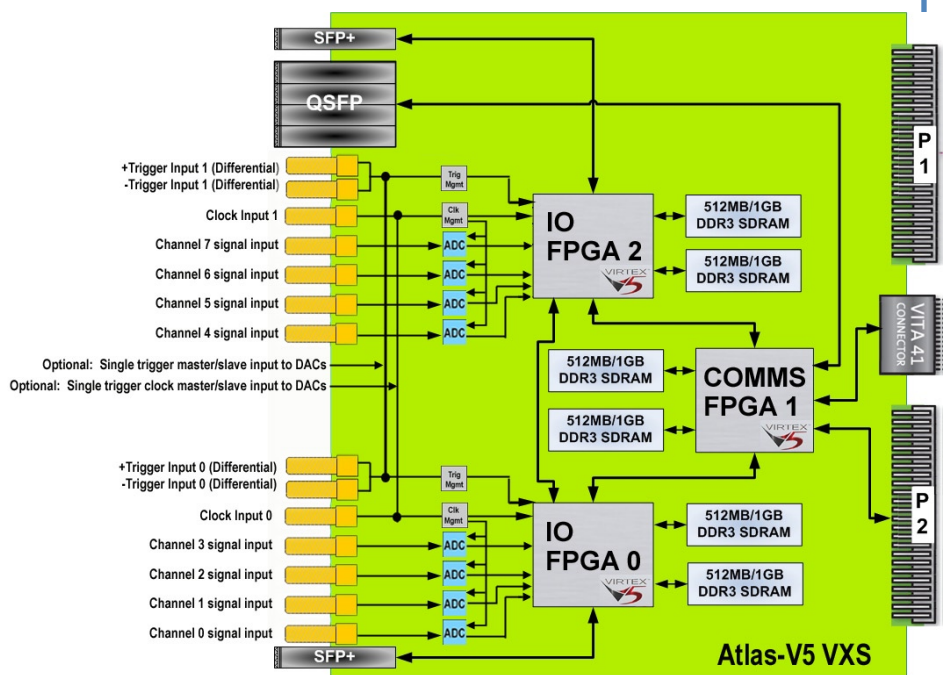
In addition to Atlas-V5, Tekmicro offers a broad range of Xilinx Virtex-5 based streaming I/O and FPGA processing solutions for both analog and digital I/O in a range of form factors.

Atlas-V5 VXS Details

ADC

Four or eight channels of up to 1 Gsps, 12-bit resolution analog to digital conversion are provided on the Atlas-V5. The inputs are single-ended, AC coupled with a full scale input level of 10 dBm (2.0 V p-p) into 50 ohms.

Atlas-V5 Configuration



Virtex-5 FPGAs

Xilinx Virtex-5 FPGAs are the heart of the Atlas-V5. The FPGAs interface between the ADCs, memory and I/O resources to provide a platform for implementing high performance real time processing. The Atlas-V5 is configured with two SX95T FPGAs and one LX110T FPGA. An LX220T, SX240T, or FX100T FPGA can be selected to match resources to the application. All FPGAs are interconnected by wide parallel LVDS busses and via high speed serial links using the Xilinx Rocket IO MGTs.

Front Panel High Speed Serial IO

Two SFP+ sites and one QSFP site are provided on the front panel which utilize standard fiber optic or 1000BaseT modules providing physical layer support for standard protocols such as Gigabit Ethernet, Serial FPDP (ANSI VITA 17.1 & 17.2), and Fibre Channel.

VXS Backplane High Speed Serial IO

The Atlas-V5 can be used as a VITA 41.0 payload card. Up to eight high speed serial links of up to 3.125 Gb/s full duplex data rates are supported via a VITA 41.0 MultiGig RT2 P0 connector. Custom or standard communication protocols can be run over these links by providing appropriate firmware in the FPGA.

QuiXstart FPGA Configuration

A number of options are available for configuring the FPGAs on the Atlas-V5. A JTAG connection is available to allow users to configure the FPGAs via standard Xilinx development tools. On board flash is available and can configure the FPGAs on power up. Tekmicro's QuiXstart tool supports flexible configuration of the FPGAs through a Gigabit Ethernet link from a remote server after a power up or reset event.

Trigger

Trigger input connections are provided on the front panel to allow the hardware to be employed in a variety of radar and EW scenarios. The trigger inputs are LVDS (LVPECL is a factory build option). Each group of four ADC channels has its own trigger input, although one trigger input may be distributed to both groups of ADCs. Multiple Atlas-V5 boards may be synchronized to within one ADC sample period using the trigger input.

Clock

Each group of four ADC channels has its own clock input although a single clock input may be distributed to all eight ADC channels (factory build option). The minimum input clock level is -6 dBm into 50 ohms.

Memory

The Atlas-V5 has two independent banks of on board double data rate (DDR3) SDRAM for each FPGA, providing a capacity of 512 MB in each bank, 1 GB total per FPGA. The on board memory can be clocked at rates up to 400 MHz, 800 MHz double data rate.

System Monitoring

The Atlas-V5 includes facilities to monitor current and temperature at various points on the board. Current monitoring of all main power rails is available. Die temperature monitoring of the three FPGAs and temperature monitoring of three locations on the PCB is also available. This allows a first level of protection when the Atlas-V5 is operating in different environmental scenarios. The output from the sensors is available to users' FPGA firmware applications, to allow the user application to adapt to changes in environmental conditions. The Atlas-V5 also uses the system monitoring sensors to implement a system protection mechanism which will, independently of the users' application, prevent excessive current or temperature from damaging the board.

PERFORMANCE SPECIFICATIONS

ADC Channels

Quantity: 4 or 8

Sampling Rate: up to 1 Gsps

Resolution: 12-bits

Type: Up to 3rd Nyquist (1.5 GHz)

Front Panel Analog Signal Input

Quantity: 8 ADC SSMC Connectors

Type: Single ended AC coupled

Full Scale Input: 0-2 V p-p (10 dBm) into 50 Ω .

Front Panel Trigger Inputs

Quantity: 1 or 2 via (2 or 4) SSMC Connectors

Type: LVDS Termination: LVDS 100 Ω differential terminated. (LVPECL as factory build option)

Mode: Optional Independent Trigger inputs for each group of four ADCs

Master/Slave: Single common trigger for all 8 ADCs

External Clock

Quantity: 1 or (2) via (2) SSMC Connectors

Single ended 50 Ω terminated

Input Power Range: -6 dBm (min) to 10 dBm (max)

Operating Modes: Clock Standalone / Master/Slave.

Standalone: Use independent clock inputs for each group of 4 ADCs

Master/Slave: Single common clock distributed to all eight ADCs

Contact factory for additional performance details.

Memory

DDR3 SDRAM (2 banks per FPGA)

Size (STD): 512 MB per bank, 1 GB total per FPGA

Bus Width: 64 bits

Speed: 400 MHz, 800 MHz double data rate

Front Panel High Speed Serial Interface

2x SFP+ Ports: Providing (2) high-speed serial connections. Range of standard protocols, including Gigabit Ethernet and FibreChannel. Firmware supplied at additional cost.

1x QSFP Port: A quadruple SFP connector, of four independent lanes of high-speed serial. The lanes may be bonded together. The port supports a range of standard protocols: Gigabit Ethernet, FibreChannel and 10-Gigabit Ethernet (via 4-lane XAUI). Firmware supplied at additional cost.

JTAG Port

Access to Virtex-5 FPGAs is available via custom JTAG cable assembly that interfaces with the JTAG programming cable.

Size: Standard 6U VMEbus board, single slot; PCB: 160mm (6.3") x 233.5mm (9.2") Option: VXS P0 connector for backplane I/O

Power: +5V, +3.3V, \pm 12V from VME64 backplane. Power consumption is dependent on customer application. Power estimating available on request.



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